APPLICATION: send a CV, a motivation letter, recommendation letters and official transcript to fabrice.seguin@telecom-bretagne.eu by 06/01/2014.

POUR CANDIDATER: envoyer CV, lettre de motivation, lettres de recommandation et relevés de notes récents à fabrice.seguin@telecom-bretagne.eu avant le 1er juin 2014.

TITLE: Analysis and design of fault tolerant computing cells in nanoscale CMOS technology.

PhD SUPERVISORS: Fabrice SEGUIN Cyril LAHUEC

UNIVERSITY: Telecom Bretagne Campus de Brest (http://www.telecom-bretagne.eu)

TEAM: Interaction Algorithme-Silicium (IAS)

KEYWORDS: Nanoscale technology, CMOS, Reliability, Noise, Integrated circuit design,

ABSTRACT:

One of the most critical challenges of the ITRS (*International Technology Roadmap for Semiconductors* 2013) is fault-tolerant computation. The increase in integration density and the requirement of low-energy consumption can only be sustained through low-powered components, with the drawback of a looser robustness against transient errors. In the near future, electronic gates processing information will be inherently unreliable.

The thesis is part of a project called RELIASIC (Reliable ASIC). In this project, we want to address this problem with a bottom-up approach, starting from an existing application (a GPS receiver) and adding some redundant mechanisms to allow the GPS receiver to be tolerant to transient errors due to low voltage supply. Our objective in RELIASIC is to produce an ASIC with two versions of the application: a standard GPS receiver and a hardened GPS receiver (a simple L1 band GPS receiver).

The main contribution of the thesis in RELIASIC project is to develop efficient et reliable error models based on low level simulations (Cadence). The goal is to characterize the impact of lowering the power on logic gates in a 28 nm CMOS technology.

In deep submicron technologies, several noise sources like random telegraph noise, thermal noise, or shot noise, must be particularly investigated and modeled. These sources should be considered in order to evaluate their impact especially when the transistors operate in sub-threshold region that is actually the case when sub-powering. Indeed, due to lower supply volt-

ages, MOS transistors will often operate in sub-threshold region in forthcoming technologies The error models will study the influence of deliberate sub-powering of integrated circuits. Based on these results, higher level simulations will be performed in order to obtain models and information about how errors appear and propagate in macro-cells. Those macro cells are critical functions of the GPS.

Besides these main tasks, the candidate will be involved in full custom designing hardened gates and functions. The latters will be implemented in the Asic design flow (CMOS 28nm) and will be consecutively tested.

Fabrice SEGUIN
Enseignant-chercheur/ Lecturer, Ph.D.
TELECOM BRETAGNE - Département Electronique
Technopôle de Brest Iroise CS 83818
29238 BREST Cedex
Tel: +33 (0)2 29 00 10 83
Fax: +33 (0)2 29 00 11 84
e-mail : fabrice.seguin@telecom-bretagne.eu
http://perso.telecom-bretagne.eu/fabriceseguin/